MODULE DESCRIPTION FORM

Module Information			
Module Title	**Analog and Digital Electronics**		**Module Delivery**
Module Type	**Basic**		☒ **Theory** ☒ **Lecture** ☒ **Lab**
Module Code	**MPH23013**		
ECTS Credits	**7 ECTS**		
SWL (hr/sem)	**175**		
Module Level	UG II	**Semester of Delivery**	3ed Semester
Administering Department	MPY	**College**	College of Sciences
Module Leader	Saja Basim Ali	**e-mail**	Saja.b@uowa.edu.iq
Module Leader's Acad. Title	**Assistant Lecturer**	**Module Leader's Qualification**	M.S.C
Module Tutor	Saja Basim Ali	**e-mail**	Saja.b@uowa.edu.iq
Peer Reviewer Name	Ahmed Musa Jaafar Othman	**e-mail**	Ahmed.mo@uowa.edu.iq
Scientific Committee Approval Date	1 – 9 - 2025	**Version Number**	1.0

Relation with other Modules			
Prerequisite module	None	**Semester**	
Co-requisites module	None	**Semester**	

Department Head Approval **Dean of the College Approval**

Module Aims, Learning Outcomes and Indicative Contents	
Module Objectives	1. To provide the student with the fundamental skills to understand the basics of semiconductors and components like diodes, transistor 2. to get experience and a fundamental comprehension of electronics. 3. The student will be able to perform the theoretical calculations necessary for analysis and design. 4. The course aims to study the basic principles of the operation of electronic circuits that contain electronic elements such as diodes of their types, transistors of their types, and methods of connection in terms of bias and arrangement. 5. the student will learn how to draw equivalent circuits for these electronic elements using different methods, 6. the student will learn how the differences between the approved methods so that the student can analyze electronic circuits. 7. To acquaint the students with the fundamental principles of two-valued logic and various devices to implement logical operations on variables. 8. Developing the student's abilities and practical skills to operate digital devices, and benefiting from them to increase individual productivity. 9. Introducing the student to the aspects of the digital electronics environment and the environment of the various devices attached to it. 10. Introducing the student to applications for multiple digital devices and information in the medical field.
Module Learning Outcomes	1. To give knowledge of some basic electronic components and circuits. 2. Identification of the structure of diode and transistor circuits. 3. Identification of NPN, PNP, JFET, and MOSFET amplifiers

	4. Able to identify and describe different analog modulation techniques 5. Describe and explain the operation of fundamental digital gates 6. Design and operate practical digital logic circuits 7. Use the basic logic gates and various digital logic circuit reduction techniques in detail. 8. Design combinational circuits. 9. Able to design and describe analog and digital logic circuits
Indicative Contents	) Theory Lectures Learning concepts of each theoretical lecture or groups of lectures. Lab. Lectures Learning concepts of each laboratory lecture or groups of lectures. Total hrs = ∑SSWL + (Mid Exam hrs+ Final Exam hrs)

Learning and Teaching Strategies	
Strategies	1. Lecture 2. Workshops 3. Laboratory sessions 4. Flipped classroom 5. Problem-based learning (PBL) 6. Peer teaching and collaborative learning 7. Reflective practice

Student Workload (SWL)			
Structured SWL (h/sem)	78	**Structured SWL (h/w)**	5.2
Unstructured SWL (h/sem)	97	**Unstructured SWL (h/w)**	6.5
Total SWL (h/sem)	**175**		

Module Evaluation

		Time/Number		Weight (Marks)		Week Due	Relevant Learning Outcome
		TH	LAB	TH	LAB		
Formative assessment	Quizzes	2	2	4	10	5 and 11	3,7
	Homework assignment	2	1	4	10	6and 13	1,8
	Onsite Assignments	-	-	-	-	Continuous	All
	Projects	1	7	2	10	14	All
Summative assessment	Midterm Exam	1		10		7	
	Final Exam	3hr		50		15	
Total assessment				100 Marks			

Delivery Plan (Weekly Syllabus)

	Material Covered
Week 1	Introduction, Insulators, conductors, semiconductors
Week 2	Intrinsic semiconductors, extrinsic semiconductors, PN-junction and applications
Week 3	Transistor, PNP, NPN, common emitter dc-analysis
Week 4	Biasing circuits, Common collector circuits, common base circuit
Week 5	FET, JFET, Output characteristic curves of JFET, JFET small signal parameters
Week 6	MOSFET
Week 7	Mid. Exam
Week 8	Introduction to digital electronics
Week 9	NUMBER SYSTEMS: Decimal & Binary system
Week 10	Binary Arithmetic
Week 11	Logic Gates and Logic Circuits
Week 12	Boolean Algebra
Week 13	Boolean Algebra and Logic Simplification
Week 14	Sequential Logic: Latches
Week 15	Flip-Flops

Delivery Plan (Weekly Lab. Syllabus)	
	Material Covered
Week 1	Static characteristic of crystal diode
Week 2	Zener diode characteristic
Week 3	Light emitting diode characteristic
Week 4	Transistor common emitting npn
Week 5	Transistor common base npn
Week 6	Half wave rectifier
Week 7	Full wave rectifier
Week 8	Introduction to Gates digital electronics
Week 9	AND Gate
Week 10	OR Gate
Week 11	NOT Gate
Week 12	NAND Gate
Week 13	NOR Gate
Week 14	The Exclusive-OR Gate
Week 15	Exclusive-NOR Gate

Learning and Teaching Resources		
	Text	**Available in the Library?**
Required Texts	ELECTRONIC PRINCIPLES, 8th Edition, 2016, McGraw-Hill Education.	No
Recommended Texts	Digital fundamentals Thomas, 11th Edition, 2015, Pearson Education.	No
Websites	https://www.talkingelectronics.com/Download/Malvino_Electronic-Principles.pdf	

Grading Scheme مخطط الدرجات				
Group	**Grade**	**Grade**	**Marks %**	**Definition**
Success Group (50 - 100)	**A -** Excellent	Excellent	90 - 100	Outstanding Performance
	B - Very Good	Very Good	80 - 89	Above average with some errors
	C - Good	Good	70 - 79	Sound work with notable errors
	D - Satisfactory	Satisfactory	60 - 69	Fair but with major shortcomings
	E - Sufficient	Sufficient	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX –** Fail	Fail	(45-49)	More work required but credit awarded
	F – Fail	Fail	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.